REMARKS

Applicant gratefully acknowledges the allowance of claims 64-68 and the Examiner's indication of allowability for claims 51-53, 60-63, 72-74, and 78. Claims 47, 48, 51, 52, 58, 60, 65, 69, and 72 have been amended. Claims 1-46 have been cancelled without prejudice to their underlying subject matter. Claims 47-78 are pending.

Claim 47 stands rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent 5,705,838 ("Jost et al."). Applicant respectfully traverses this rejection.

Claim 47 defines a memory device and recites "a first conductive stud and a second conductive stud" and "an interconnect line over and in electrical contact with said first conductive stud, wherein a portion of said interconnect line overlays a portion of said second conductive stud" and "an insulating sidewall separating said interconnect line from said second conductive stud." Such a device is not disclosed by Jost et al.

Jost et al. fails to disclose a second conductive stud, as recited by the claim. Jost et al. discloses a DRAM cell. The feature 38 alleged to be a "second conductive silicon-containing stud" (Office Action at 2) is not, but is actually a bottom electrode of a capacitor of the DRAM cell. The Jost et al. specification does not suggest that this bottom electrode 38 has any portion that could be considered a stud (col. 4, first paragraph); the device shown in figure 5 also has no stud portion for the capacitor 44. Also, Jost et al. fails to disclose "an insulating sidewall separating said interconnect line from said second conductive stud." Assuming arguendo that the capacitor bottom electrode (38) of Jost et al. could be considered a stud (which it cannot), no sidewall separates it from the bit line. For either and both of the above reasons, Jost et al. does

not anticipate independent claim 47 and the rejection under 35 U.S.C. § 102(b) thereof is respectfully requested to be withdrawn.

Claims 48-50 and 54-59 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Jost et al. in view of U.S. Patent 6,188,112 ("Bryant") and U.S. Patent 6,069,060 ("Matsumoto"). Applicant respectfully traverses this rejection.

Claims 48-50 and 54-57 depend from independent claim 47, which, as discussed above, is patentable over Jost et al. Regardless of what Bryant and Matsumoto disclose regarding the use of epitaxial silicon in memory devices, about which Applicant makes no comment, these references cannot supplement Jost et al. to remedy its deficiencies with regard to the subject matter recited by claim 47. Therefore, independent claim 47 and dependent claims 48-50 and 54-57 are patentable over Jost et al., Bryant, and Matsumoto and Applicant respectfully requests that the 35 U.S.C. § 103(a) rejection of these claims be withdrawn.

Claim 58, as amended, defines a DRAM cell structure and recites "an access transistor with source and drain areas" and "a first conductive epitaxial silicon stud and a second conductive epitaxial silicon stud each in contact with a respective one of said source and drain areas of said access transistor" and "a bit line over and in electrical contact with said first conductive epitaxial silicon stud, wherein at least a portion of said bit line overlays a portion of said second conductive epitaxial silicon stud" and "an insulating sidewall structure separating said bit line from said second conductive epitaxial silicon stud." This claimed device is not taught or suggested by Jost et al., Bryant, and Matsumoto.

As discussed above in relation to the patentability of independent claim 47 and the claims depending therefrom, none of the references teaches or suggests the recited first and second studs or the insulating sidewall structure of the claims. Therefore, for at least the same reasoning set forth above, independent claim 58 and dependent claim 59 are patentable over the cited references. Applicant respectfully requests that the 35 U.S.C. § 103(a) rejection of claims 58 and 59 be withdrawn.

Claims 69-71 and 75-77 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Jost et al. in view of Bryant and Matsumoto and also in view of U.S. Patent 6,051,509 ("Tsuchiaki"). Applicant respectfully traverses this rejection.

Claim 69, as amended, defines a processor-based system having a processor and a memory circuit and recites "a first conductive epitaxial silicon stud and a second conductive epitaxial silicon stud" and "an interconnect line over and in electrical contact with said first conductive stud, wherein a portion of said interconnect line overlays a portion of said second conductive epitaxial silicon stud" and "an insulating sidewall structure separating said interconnect line from said second conductive epitaxial silicon stud." As discussed above in relation to the patentability of independent claim 47 and the claims depending therefrom, none of Jost et al., Bryant, and Matsumoto teaches or suggests the recited first and second studs or the insulating sidewall structure of the claims; Tsuchiaki cannot remedy these deficiencies as it likewise fails to teach or suggest such subject matter. Therefore, for at least the same reasoning set forth above for other independent claims, independent claim 69 and dependent claims 70, 71, and 75-77 are patentable over the cited references. Applicant respectfully requests that the 35 U.S.C. § 103(a) rejection of claims 69-71 and 75-77 be withdrawn.

Applicant believes all pending claims are in immediate condition for allowance and respectfully requests a Notice of Allowance for all pending claims (47-78).

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Respectfully submitted,

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